Search History

STN
(HCAPLUS, INSPEC, CAPLUS, ZCAPLAIL)
5/5/05

=> d l9 1-22 abs,bib

L9 ANSWER 1 OF 22 HCAPLUS COPYRIGHT 2005 ACS on STN

AB The invention relates to a process for making a low-defect, substantially relaxed **SiGe**-on-**insulator substrate** material. The method includes first forming a **Ge**-containing **layer** on a **surface** of a first single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to Ge diffusion. A **heating** step is then performed at a temperature that approaches the m.p. of the final **SiGe** alloy and retards the formation of stacking fault defects while retaining Ge. The **heating** step permits interdiffusion of Ge throughout the first single crystal **Si layer** and the Ge-containing **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Moreover, because the **heating** step is carried out at a temperature that approaches the m.p. of the final **SiGe** alloy, defects that persist in the single crystal **SiGe** layer as a result of relaxation are efficiently annihilated therefrom. In one embodiment, the **heating** step includes an oxidation process that is performed at a temperature from about 1230° to about 1320°, for a time period of less than about 2 h. This embodiment provides SGOI substrate that have minimal surface pitting and reduced crosshatching.

AN 2004:1127015 HCAPLUS

DN 142:84452

TI Fabrication of a SGOI wafer by **annealing** near the alloy m.p.

IN Bedell, Stephen W.; Chen, Huajie; Domenicucci, Anthony G.; Fogel, Keith E.; Murphy, Richard J.; Sadana, Devendra K.

PA International Business Machines Corporation, USA

SO U.S. Pat. Appl. Publ., 22 pp., Cont.-in-part of U.S. Ser. No. 448,948.
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004259334	A1	20041223	US 2004-855915	20040527
	US 2004238885	A1	20041202	US 2003-448948	20030530
PRAI	US 2003-448948	A2	20030530		

L9 ANSWER 2 OF 22 HCAPLUS COPYRIGHT 2005 ACS on STN

AB A method of forming a substantially relaxed, high-quality **SiGe**-on-**insulator substrate** material using SIMOX and Ge interdiffusion is provided. The method includes 1st implanting ions into a Si-containing substrate to form an implant rich region in the Si-containing substrate. The implant rich region has a sufficient ion concentration such that during a subsequent **anneal** at high temps. a **barrier layer** that is **resistant** to Ge diffusion is formed. Next, a **Ge**-containing **layer** is formed on a **surface** of the **Si**-containing substrate, and thereafter a **heating** step was performed at a temperature which permits formation of the barrier layer and interdiffusion of Ge thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer.

AN 2004:1036489 HCAPLUS

DN 142:31431

TI Formation of **silicon-germanium**-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion **anneal**

IN Bedell, Stephen W.; De Souza, Joel P.; Fogel, Keith E.; Sadana, Devendra K.; Shahidi, Ghavam G.

PA International Business Machines Corporation, USA

SO U.S. Pat. Appl. Publ., 18 pp., Cont.-in-part of U.S. Ser. No. 448,947.
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 3

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE

PI	US 2004241460	A1	20041202	US 2003-696601	20031029
	US 6861158	B2	20050301		
	US 2004241459	A1	20041202	US 2003-448947	20030530
	US 6855436	B2	20050215		
PRAI	US 2003-448947	A2	20030530		

L9 ANSWER 3 OF 22 HCAPLUS COPYRIGHT 2005 ACS on STN

AB A method of forming a substantially relaxed, high-quality **SiGe** -on-**insulator substrate** material using SIMOX and Ge interdiffusion is provided. The method includes 1st implanting ions into a Si-containing substrate to form an implant rich region in the Si-containing substrate. The implant rich region has a sufficient ion concentration such that during a subsequent **anneal** at high temps. a **barrier layer** that is **resistant** to Ge diffusion is formed. Next, a **Ge**-containing **layer** is formed on a **surface** of the **Si**-containing substrate, and thereafter a **heating** step was performed at a temperature which permits formation of the barrier layer and interdiffusion of Ge thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer.

AN 2004:1036488 HCAPLUS

DN 142:31430

TI Formation of **silicon-germanium**-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion **anneal**

IN Bedell, Stephen W.; Fogel, Keith E.; Sadana, Devendra K.; Shahidi, Ghavam G.

PA International Business Machines Corporation, USA

SO U.S. Pat. Appl. Publ., 12 pp.
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 3

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004241459	A1	20041202	US 2003-448947	20030530
	US 6855436	B2	20050215		
	US 2004241460	A1	20041202	US 2003-696601	20031029
	US 6861158	B2	20050301		
	JP 2004363592	A2	20041224	JP 2004-158994	20040528
	US 2005090080	A1	20050428	US 2004-993270	20041119
PRAI	US 2001-861590	A3	20010521		
	US 2003-448947	A2	20030530		

L9 ANSWER 4 OF 22 HCAPLUS COPYRIGHT 2005 ACS on STN

AB A method of forming a low-defect, substantially relaxed **SiGe**-on-**insulator substrate** material is provided. The method includes 1st forming a **Ge**-containing **layer** on a **surface** of a 1st single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to Ge diffusion. A **heating** step is then performed at a temperature that approaches the m.p. of the final **SiGe** alloy and retards the formation of stacking fault defects while retaining Ge. The **heating** step permits interdiffusion of Ge throughout the 1st single crystal **Si layer** and the Ge-containing **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Also, because the **heating** step is carried out at a temperature that approaches the m.p. of the final **SiGe** alloy, defects that persist in the single crystal **SiGe** layer as a result of relaxation are efficiently annihilated therefrom.

AN 2004:1036304 HCAPLUS

DN 142:31408

TI High-quality SGOI by oxidation near the alloy melting temperature

IN Bedell, Stephen W.; Domenicucci, Anthony G.; Fogel, Keith E.; Sadana, Devendra K.

PA International Business Machines Corporation, USA

SO U.S. Pat. Appl. Publ., 17 pp.
CODEN: USXXCO

DT Patent

LA English
FAN.CNT 2

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004238885	A1	20041202	US 2003-448948	20030530
	US 2004259334	A1	20041223	US 2004-855915	20040527
	WO 2004112102	A2	20041223	WO 2004-US16747	20040527
	WO 2004112102	A3	20050224		

W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW

RW: BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG

PRAI US 2003-448948 A2 20030530

L9 ANSWER 5 OF 22 HCAPLUS COPYRIGHT 2005 ACS on STN

AB A method of forming a relaxed **Si-Ge**-on-**insulator substrate** having enhanced relaxation, significantly lower defect d. and improved surface quality is provided. The method includes forming a **Si-Ge** alloy **layer** on a **surface** of a 1st single crystal **Si layer**. The 1st single crystal **Si layer** has an interface with an underlying **barrier layer** that is **resistant** to Ge diffusion. Next, ions that are capable of forming defects that allow mech. decoupling at or near said interface are implanted into the structure and thereafter the structure including the implanted ions is subjected to a **heating** step which permits interdiffusion of Ge throughout the 1st single crystal **Si layer** and the **Si-Ge layer** to form a substantially relaxed, single crystal and homogeneous **Si-Ge layer** atop the barrier **layer**. **Si-Ge**-on-**insulator substrates** having the improved properties as well as heterostructures containing the same are also provided.

AN 2004:59492 HCAPLUS

DN 140:121000

TI Use of implantation to improve material properties of **silicon-germanium**-on-insulator material made by thermal diffusion

IN Bedell, Stephen W.; Fogel, Keith E.; Sadana, Devendra K.

PA International Business Machines Corporation, USA

SO U.S. Pat. Appl. Publ., 15 pp.
CODEN: USXXCO

DT Patent

LA English

FAN.CNT 1

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 2004012075	A1	20040122	US 2002-196611	20020716
	US 6841457	B2	20050111		
	JP 2004040122	A2	20040205	JP 2003-274987	20030715
PRAI	US 2002-196611	A	20020716		

L9 ANSWER 6 OF 22 HCAPLUS COPYRIGHT 2005 ACS on STN

AB A method of forming a thin, high-quality relaxed **SiGe**-on-**insulator substrate** material is provided which first includes forming a **SiGe** or pure **Ge layer** on a **surface** of a first single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to the diffusion of Ge. Optionally forming a **Si** cap **layer** over the **SiGe** or pure Ge **layer**, and thereafter **heating** the various layers at a temperature which permits interdiffusion of Ge throughout the first single crystal

Si layer, the optional **Si** cap and the **SiGe** or pure Ge **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Addnl. **SiGe** regrowth and/or formation of a strained epi-**Si layer** may follow the above steps. **SiGe**-on-**insulator substrate** materials as well as structures including at least the **SiGe**-on-**insulator substrate** materials are also disclosed herein.

AN 2003:570576 HCAPLUS
DN 139:109897
TI Method of creating high-quality relaxed **SiGe**-on-insulator for strained Si CMOS applications
IN Bedell, Stephen W.; Chu, Jack O.; Fogel, Keith E.; Koester, Steven J.; Sadana, Devendra K.; Ott, John A.
PA International Business Machines Corporation, USA
SO U.S. Pat. Appl. Publ., 11 pp.
CODEN: USXXCO
DT Patent
LA English
FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI US 2003139000	A1	20030724	US 2002-55138	20020123
US 6805962	B2	20041019		
WO 2003063229	A1	20030731	WO 2003-US1431	20030116
W: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW				
RW: GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW, AM, AZ, BY, KG, KZ, MD, RU, TJ, TM, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IT, LU, MC, NL, PT, SE, SI, SK, TR, BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG				
EP 1479103	A1	20041124	EP 2003-731957	20030116
R: AT, BE, CH, DE, DK, ES, FR, GB, GR, IT, LI, LU, NL, SE, MC, PT, IE, SI, LT, LV, FI, RO, MK, CY, AL, TR, BG, CZ, EE, HU, SK				
US 2004192069	A1	20040930	US 2004-824289	20040414
PRAI US 2002-55138	A	20020123		
WO 2003-US1431	W	20030116		

RE.CNT 10 THERE ARE 10 CITED REFERENCES AVAILABLE FOR THIS RECORD
ALL CITATIONS AVAILABLE IN THE RE FORMAT

L9 ANSWER 7 OF 22 USPATFULL on STN
AB High-quality, metastable **SiGe** alloys are formed on SOI substrates having an SOI layer of about 500 Å or less, the **SiGe** layers can remain substantially fully strained compared to identical **SiGe** layers formed on thicker SOI substrates and subsequently **annealed** and/or oxidized at high temperatures. The present invention thus provides a method of `frustrating` metastable strained **SiGe** layers by growing them on thin, clean and high-quality SOI substrates.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2005:56863 USPATFULL
TI Use of thin SOI to inhibit relaxation of **SiGe** layers
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Chen, Huajie, Wappingers Falls, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
PA INTERNATIONAL BUSINESS MACHINES CORPORATION, ARMONK, NY (U.S. corporation)
PI US 2005048778 A1 20050303
AI US 2003-654232 A1 20030903 (10)
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY,

NY, 11530
CLMN Number of Claims: 30
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 602
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 8 OF 22 USPATFULL on STN
AB A method of fabricating high-quality, substantially relaxed **SiGe** -on-**insulator substrate** materials which may be used as a template for strained Si is described. A silicon-on-**insulator substrate** with a very thin top **Si layer** is used as a template for compressively strained **SiGe** growth. Upon relaxation of the **SiGe** layer at a sufficient temperature, the nature of the dislocation motion is such that the strain-relieving defects move downward into the thin **Si layer** when the buried oxide behaves semi-viscously. The thin **Si layer** is consumed by oxidation of the buried oxide/thin Si interface. This can be accomplished by using internal oxidation at high temperatures. In this way the role of the original thin **Si layer** is to act as a sacrificial defect sink during relaxation of the **SiGe** alloy that can later be consumed using internal oxidation.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2005:4126 USPATFULL
TI Defect reduction by oxidation of silicon
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Chen, Huajie, Wappingers Falls, NY, UNITED STATES
Domenicucci, Anthony G., New Paltz, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
PA INTERNATIONAL BUSINESS MACHINES CORPORATION, ARMONK, NY (U.S. corporation)
PI US 2005003229 A1 20050106
AI US 2003-610612 A1 20030701 (10)
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 33
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 693
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 9 OF 22 USPATFULL on STN
AB A method of forming a low-defect, substantially relaxed **SiGe** -on-**insulator substrate** material is provided. The method includes first forming a **Ge**-containing **layer** on a **surface** of a first single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to Ge diffusion. A **heating** step is then performed at a temperature that approaches the melting point of the final **SiGe** alloy and retards the formation of stacking fault defects while retaining Ge. The **heating** step permits interdiffusion of Ge throughout the first single crystal **Si layer** and the Ge-containing **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Moreover, because the **heating** step is carried out at a temperature that approaches the melting point of the final **SiGe** alloy, defects that persist in the single crystal **SiGe** layer as a result of relaxation are efficiently annihilated therefrom. In one embodiment, the **heating** step includes an oxidation process that is performed at a temperature from about 1230° to about 1320° C. for a time period of less than about 2 hours. This embodiment provides SGOI substrate that have minimal surface pitting and reduced crosshatching.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:327514 USPATFULL
TI High-quality SGOI by **annealing** near the alloy melting point
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Chen, Huajie, UNITED STATES
Domenicucci, Anthony G., New Paltz, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Murphy, Richard J., Clinton Corners, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
PA INTERNATIONAL BUSINESS MACHINES CORPORATION, ARMONK, NY (U.S. corporation)
PI US 2004259334 A1 20041223
AI US 2004-855915 A1 20040527 (10)
RLI Continuation-in-part of Ser. No. US 2003-448948, filed on 30 May 2003, PENDING
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 58
ECL Exemplary Claim: 1
DRWN 12 Drawing Page(s)
LN.CNT 952
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 10 OF 22 USPATFULL on STN
AB The present invention provides a method of fabricating a **SiGe**-on-**insulator substrate** in which lattice engineering is employed to decouple the interdependence between **SiGe** thickness, Ge fraction and strain relaxation. The method includes providing a **SiGe**-on-**insulator substrate** material comprising a **SiGe** alloy layer having a selected in-plane lattice parameter, a selected thickness parameter and a selected Ge content parameter, wherein the selected in-plane lattice parameter has a constant value and one or both of the other parameters, i.e., thickness or Ge content, have adjustable values; and adjusting one or both of the other parameters to final selected values, while maintaining the selected in-plane lattice parameter. The adjusting is achieved utilizing either a thinning process or a thermal dilution process depending on which parameters are fixed and which are adjustable.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:307335 USPATFULL
TI **SiGe** lattice engineering using a combination of oxidation, thinning and epitaxial regrowth
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Chen, Huajie, Wappingers Falls, NY, UNITED STATES
Fogel, Keith E., Mohegan lake, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
PA International Business Machines Corporation, Armonk, NY (U.S. corporation)
PI US 2004242006 A1 20041202
AI US 2003-448954 A1 20030530 (10)
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 18
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 711
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 11 OF 22 USPATFULL on STN
AB A method of forming a substantially relaxed, high-quality **SiGe**-on-**insulator substrate** material using SIMOX and Ge

interdiffusion is provided. The method includes first implanting ions into a Si-containing substrate to form an implanted-ion rich region in the Si-containing substrate. The implanted-ion rich region has a sufficient ion concentration such that during a subsequent **anneal** at high temperatures a **barrier layer** that is **resistant** to Ge diffusion is formed. Next, a **Ge**-containing **layer** is formed on a **surface** of the **Si**-containing substrate, and thereafter a **heating** step is performed at a temperature which permits formation of the barrier layer and interdiffusion of Ge thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:306791 USPATFULL
TI Formation of **silicon-Germanium**-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion **anneal**
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
de Souza, Joel P., Putnam Valley, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
Shahidi, Ghavam G., Pound Ridge, NY, UNITED STATES
PA INTERNATIONAL BUSINESS MACHINES CORPORATION, ARMONK, NY (U.S. corporation)
PI US 2004241460 A1 20041202
US 6861158 B2 20050301
AI US 2003-696601 A1 20031029 (10)
RLI Continuation-in-part of Ser. No. US 2003-448947, filed on 30 May 2003, PENDING
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 47
ECL Exemplary Claim: CLM-01-38
DRWN 7 Drawing Page(s)
LN.CNT 1052
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 12 OF 22 USPATFULL on STN
AB A method of forming a substantially relaxed, high-quality **SiGe**-on-**insulator substrate** material using SIMOX and Ge interdiffusion is provided. The method includes first implanting ions into a Si-containing substrate to form an implant rich region in the Si-containing substrate. The implant rich region has a sufficient ion concentration such that during a subsequent **anneal** at high temperatures a **barrier layer** that is **resistant** to Ge diffusion is formed. Next, a **Ge**-containing **layer** is formed on a **surface** of the **Si**-containing substrate, and thereafter a **heating** step is performed at a temperature which permits formation of the barrier layer and interdiffusion of Ge thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:306790 USPATFULL
TI Formation of **silicon-germanium**-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion **anneal**
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
Shahidi, Ghavam G., Pound Ridge, NY, UNITED STATES
PA International Business Machines Corporation, Armonk, NY (U.S. corporation)
PI US 2004241459 A1 20041202
US 6855436 B2 20050215
AI US 2003-448947 A1 20030530 (10)
DT Utility

FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 38
ECL Exemplary Claim: 1
DRWN 5 Drawing Page(s)
LN.CNT 656
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 13 OF 22 USPATFULL on STN
AB A method of forming a low-defect, substantially relaxed **SiGe**-on-**insulator substrate** material is provided. The method includes first forming a **Ge**-containing **layer** on a **surface** of a first single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to Ge diffusion. A **heating** step is then performed at a temperature that approaches the melting point of the final **SiGe** alloy and retards the formation of stacking fault defects while retaining Ge. The **heating** step permits interdiffusion of Ge throughout the first single crystal **Si layer** and the Ge-containing **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Moreover, because the **heating** step is carried out at a temperature that approaches the melting point of the final **SiGe** alloy, defects that persist in the single crystal **SiGe** layer as a result of relaxation are efficiently annihilated therefrom.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:304230 USPATFULL
TI High-quality SGOI by oxidation near the alloy melting temperature
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Domenicucci, Anthony G., New Paltz, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
PA International Business Machines Corporation, Armonk, NY (U.S. corporation)
PI US 2004238885 A1 20041202
AI US 2003-448948 A1 20030530 (10)
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 47
ECL Exemplary Claim: 1
DRWN 9 Drawing Page(s)
LN.CNT 785
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 14 OF 22 USPATFULL on STN
AB A method of forming a thin, high-quality relaxed **SiGe**-on-**insulator substrate** material is provided which first includes forming a **SiGe** or pure **Ge layer** on a **surface** of a first single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to the diffusion of Ge. Optionally forming a **Si** cap **layer** over the **SiGe** or pure Ge **layer**, and thereafter **heating** the various layers at a temperature which permits interdiffusion of Ge throughout the first single crystal **Si layer**, the optional **Si** cap and the **SiGe** or pure Ge **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Additional **SiGe** regrowth and/or formation of a strained epi-**Si layer** may follow the above steps. **SiGe**-on-**insulator substrate** materials as well as structures including at least the **SiGe**-on-**insulator substrate** materials are also disclosed herein.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:247472 USPATFULL
TI Method of creating high-quality relaxed **SiGe**-on-insulator for strained Si CMOS applications
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Chu, Jack O., Manhasset Hills, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Koester, Steven J., Ossining, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
PA International Business Machines Corporation, Armonk, NY (U.S. corporation)
PI US 2004192069 A1 20040930
AI US 2004-824289 A1 20040414 (10)
RLI Division of Ser. No. US 2002-55138, filed on 23 Jan 2002, PENDING
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 35
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 515
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 15 OF 22 USPATFULL on STN
AB Thermal mixing methods of forming a substantially relaxed and low-defect SGOI substrate material are provided. The methods include a patterning step which is used to form a structure containing at least **SiGe** islands formed atop a Ge **resistant** diffusion **barrier layer**. Patterning of the **SiGe** layer into islands changes the local forces acting at each of the island edges in such a way so that the relaxation force is greater than the forces that oppose relaxation. The absence of restoring forces at the edges of the patterned layers allows the final **SiGe** film to relax further than it would if the film was continuous.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:124793 USPATFULL
TI Relaxed, low-defect SGOI for strained Si CMOS applications
IN Agnello, Paul D., Wappingers Falls, NY, UNITED STATES
Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Dennard, Robert H., New Rochelle, NY, UNITED STATES
Domenicucci, Anthony G., New Paltz, NY, UNITED STATES
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PA INTERNATIONAL BUSINESS MACHINES CORPORATION, ARMONK, NY, UNITED STATES (non-U.S. corporation)
PI US 2004094763 A1 20040520
AI US 2002-300189 A1 20021120 (10)
DT Utility
FS APPLICATION
LREP SCULLY SCOTT MURPHY & PRESSER, PC, 400 GARDEN CITY PLAZA, GARDEN CITY, NY, 11530
CLMN Number of Claims: 66
ECL Exemplary Claim: 1
DRWN 6 Drawing Page(s)
LN.CNT 986
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 16 OF 22 USPATFULL on STN
AB A method of forming a relaxed **SiGe**-on-**insulator substrate** having enhanced relaxation, significantly lower defect density and improved surface quality is provided. The method includes forming a **SiGe** alloy **layer** on a surface of a first single crystal **Si layer**. The first single crystal **Si layer** has an interface with an underlying **barrier layer** that is **resistant** to Ge

diffusion. Next, ions that are capable of forming defects that allow mechanical decoupling at or near said interface are implanted into the structure and thereafter the structure including the implanted ions is subjected to a **heating** step which permits interdiffusion of Ge throughout the first single crystal **Si layer** and the **SiGe layer** to form a substantially relaxed, single crystal and homogeneous **SiGe** layer atop the barrier layer. **SiGe**-on-**insulator substrates** having the improved properties as well as heterostructures containing the same are also provided.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:16778 USPATFULL
TI Use of hydrogen implantation to improve material properties of **silicon-germanium**-on-insulator material made by thermal diffusion
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
PA INTERNATIONAL BUSINESS MACHINES CORPORATION, Armonk, NY, UNITED STATES (U.S. corporation)
PI US 2004012075 A1 20040122
US 6841457 B2 20050111
AI US 2002-196611 A1 20020716 (10)
DT Utility
FS APPLICATION
LREP Steven Fischman, Scully, Scott,, Murphy & Presser, 400 Garden City Plaza, Garden City, NY, 11530
CLMN Number of Claims: 41
ECL Exemplary Claim: 1
DRWN 7 Drawing Page(s)
LN.CNT 766
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 17 OF 22 USPATFULL on STN
AB A method of forming a thin, high-quality relaxed **SiGe**-on-**insulator substrate** material is provided which first includes forming a **SiGe** or pure **Ge layer** on a **surface** of a first single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to the diffusion of Ge. Optionally forming a **Si** cap **layer** over the **SiGe** or pure Ge **layer**, and thereafter **heating** the various layers at a temperature which permits interdiffusion of Ge throughout the first single crystal **Si layer**, the optional **Si** cap and the **SiGe** or pure Ge **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Additional **SiGe** regrowth and/or formation of a strained epi-**Si layer** may follow the above steps. **SiGe**-on-**insulator substrate** materials as well as structures including at least the **SiGe**-on-**insulator substrate** materials are also disclosed herein.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:201015 USPATFULL
TI Method of creating high-quality relaxed **SiGe**-on-insulator for strained Si CMOS applications
IN Bedell, Stephen W., Wappingers Falls, NY, UNITED STATES
Chu, Jack O., Manhasset Hills, NY, UNITED STATES
Fogel, Keith E., Mohegan Lake, NY, UNITED STATES
Koester, Steven J., Ossining, NY, UNITED STATES
Sadana, Devendra K., Pleasantville, NY, UNITED STATES
OTT, John A, GREENWOOD LAKE, NY, UNITED STATES
PA INTERNATIONAL BUSINESS MACHINES CORPORATION, ARMONK, NY (U.S. corporation)
PI US 2003139000 A1 20030724
US 6805962 B2 20041019

AI US 2002-55138 A1 20020123 (10)
DT Utility
FS APPLICATION
LREP Steven Fischman, Scully, Scott, Murphy & Presser, 400 Garden City Plaza, Garden City, NY, 11530
CLMN Number of Claims: 56
ECL Exemplary Claim: 1
DRWN 4 Drawing Page(s)
LN.CNT 582
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 18 OF 22 USPATFULL on STN
AB A silicon oxide film and a doped polysilicon film are successively formed on a silicon substrate. Then, a doped polysilicon-germanium film is formed on the doped polysilicon film as a film having a higher impurity activation rate than polysilicon. Then, a barrier film, a metal film and another barrier film are successively formed on the doped polysilicon-germanium film. Thus obtained is a method of manufacturing a semiconductor device comprising a polymetal gate capable of suppressing increase of gate resistance also when an impurity introduced into a semiconductor film diffuses into the barrier films.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2002:268664 USPATFULL
TI Method of manufacturing semiconductor device
IN Kunikiyo, Tatsuya, Tokyo, JAPAN
PA Mitsubishi Denki Kabushiki Kaisha, Tokyo, JAPAN (non-U.S. corporation)
PI US 6465335 B1 20021015
AI US 2000-690836 20001018 (9)
PRAI JP 2000-143277 20000516
DT Utility
FS GRANTED
EXNAM Primary Examiner: Nguyen, Tuan H.; Assistant Examiner: Nguyen, Thanh
LREP Oblon, Spivak, McClelland, Maier & Neustadt, P.C.
CLMN Number of Claims: 7
ECL Exemplary Claim: 1
DRWN 29 Drawing Figure(s); 25 Drawing Page(s)
LN.CNT 1044
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 19 OF 22 USPAT2 on STN
AB A method of forming a substantially relaxed, high-quality **SiGe** -on-**insulator substrate** material using SIMOX and Ge interdiffusion is provided. The method includes first implanting ions into a Si-containing substrate to form an implanted-ion rich region in the Si-containing substrate. The implanted-ion rich region has a sufficient ion concentration such that during a subsequent **anneal** at high temperatures a **barrier layer** that is **resistant** to Ge diffusion is formed. Next, a **Ge**-containing **layer** is formed on a **surface** of the **Si**-containing substrate, and thereafter a **heating** step is performed at a temperature which permits formation of the barrier layer and interdiffusion of Ge thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:306791 USPAT2
TI Formation of **silicon-germanium**-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion **anneal**
IN Bedell, Stephen W., Wappingers Falls, NY, United States
de Souza, Joel P., Putnam Valley, NY, United States
Fogel, Keith E., Mohegan Lake, NY, United States
Sadana, Devendra K., Pleasantville, NY, United States
Shahidi, Ghavam G., Pound Ridge, NY, United States
PA International Business Machines Corporation, Armonk, NY, United States (U.S. corporation)
PI US 6861158 B2 20050301

AI US 2003-696601 20031029 (10)
RLI Continuation-in-part of Ser. No. US 2003-448947, filed on 30 May 2003
DT Utility
FS GRANTED
EXNAM Primary Examiner: Stein, Stephen
LREP Scully, Scott, Murphy & Presser, Trepp, Esq., Robert M.
CLMN Number of Claims: 13
ECL Exemplary Claim: 1
DRWN 15 Drawing Figure(s); 7 Drawing Page(s)
LN.CNT 912
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 20 OF 22 USPAT2 on STN
AB A method of forming a substantially relaxed, high-quality **SiGe** -on-**insulator substrate** material using SIMOX and Ge interdiffusion is provided. The method includes first implanting ions into a Si-containing substrate to form an implant rich region in the Si-containing substrate. The implant rich region has a sufficient ion concentration such that during a subsequent **anneal** at high temperatures a **barrier layer** that is **resistant** to Ge diffusion is formed. Next, a **Ge** -containing **layer** is formed on a **surface** of the **Si**-containing substrate, and thereafter a **heating** step is performed at a temperature which permits formation of the barrier layer and interdiffusion of Ge thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:306790 USPAT2
TI Formation of **silicon-germanium**-on-insulator (SGOI) by an integral high temperature SIMOX-Ge interdiffusion **anneal**
IN Bedell, Stephen W., Wappingers Falls, NY, United States
Fogel, Keith E., Mohegan Lake, NY, United States
Sadana, Devendra K., Pleasantville, NY, United States
Shahidi, Ghavam G., Pound Ridge, NY, United States
PA International Business Machines Corporation, Armonk, NY, United States (U.S. corporation)
PI US 6855436 B2 20050215
AI US 2003-448947 20030530 (10)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Stein, Stephen
LREP Scully, Scott, Murphy & Presser, Trepp, Esq., Robert M.
CLMN Number of Claims: 11
ECL Exemplary Claim: 5
DRWN 13 Drawing Figure(s); 5 Drawing Page(s)
LN.CNT 557
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 21 OF 22 USPAT2 on STN
AB A method of forming a relaxed **SiGe**-on-**insulator substrate** having enhanced relaxation, significantly lower defect density and improved surface quality is provided. The method includes forming a **SiGe** alloy **layer** on a surface of a first single crystal **Si layer**. The first single crystal **Si layer** has an interface with an underlying **barrier layer** that is **resistant** to Ge diffusion. Next, ions that are capable of forming defects that allow mechanical decoupling at or near said interface are implanted into the structure and thereafter the structure including the implanted ions is subjected to a **heating** step which permits interdiffusion of Ge throughout the first single crystal **Si layer** and the **SiGe layer** to form a substantially relaxed, single crystal and homogeneous **SiGe** layer atop the barrier layer. **SiGe**-on-**insulator substrates** having the improved properties as well as heterostructures containing the same are also provided.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2004:16778 USPAT2
TI Use of hydrogen implantation to improve material properties of **silicon-germanium**-on-insulator material made by thermal diffusion
IN Bedell, Stephen W., Wappingers Falls, NY, United States
Fogel, Keith E., Mohegan Lake, NY, United States
Sadana, Devendra K., Pleasantville, NY, United States
PA International Business Machines Corporation, Armonk, NY, United States (U.S. corporation)
PI US 6841457 B2 20050111
AI US 2002-196611 20020716 (10)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Niebling, John F.; Assistant Examiner: Isaac, Stanetta
LREP Scully, Scott, Murphy & Presser, Trepp, Esq., Robert M.
CLMN Number of Claims: 29
ECL Exemplary Claim: 1
DRWN 14 Drawing Figure(s); 6 Drawing Page(s)
LN.CNT 704
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

L9 ANSWER 22 OF 22 USPAT2 on STN
AB A method of forming a thin, high-quality relaxed **SiGe**-on-**insulator substrate** material is provided which first includes forming a **SiGe** or pure **Ge layer** on a **surface** of a first single crystal **Si layer** which is present atop a **barrier layer** that is **resistant** to the diffusion of Ge. Optionally forming a **Si** cap **layer** over the **SiGe** or pure Ge **layer**, and thereafter **heating** the various layers at a temperature which permits interdiffusion of Ge throughout the first single crystal **Si layer**, the optional **Si** cap and the **SiGe** or pure Ge **layer** thereby forming a substantially relaxed, single crystal **SiGe** layer atop the barrier layer. Additional **SiGe** regrowth and/or formation of a strained epi-**Si layer** may follow the above steps. **SiGe**-on-**insulator substrate** materials as well as structures including at least the **SiGe**-on-**insulator substrate** materials are also disclosed herein.

CAS INDEXING IS AVAILABLE FOR THIS PATENT.
AN 2003:201015 USPAT2
TI Method of creating high-quality relaxed **SiGe**-on-insulator for strained Si CMOS applications
IN Bedell, Stephen W., Wappingers Falls, NY, United States
Chu, Jack O., Manhasset Hills, NY, United States
Fogel, Keith E., Mohegan Lake, NY, United States
Koester, Steven J., Ossining, NY, United States
Sadana, Devendra K., Pleasantville, NY, United States
Ott, John Albrecht, Greenwood Lake, NY, United States
PA International Business Machines Corporation, Armonk, NY, United States (U.S. corporation)
PI US 6805962 B2 20041019
AI US 2002-55138 20020123 (10)
DT Utility
FS GRANTED
EXNAM Primary Examiner: Stein, Stephen
LREP Scully, Scott, Murphy & Presser, Trepp, Robert M.
CLMN Number of Claims: 22
ECL Exemplary Claim: 1
DRWN 12 Drawing Figure(s); 4 Drawing Page(s)
LN.CNT 484
CAS INDEXING IS AVAILABLE FOR THIS PATENT.

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(FILE 'HOME' ENTERED AT 10:20:52 ON 04 MAY 2005)

FILE 'HCAPLUS, INSPEC, JAPIO, USPATFULL, USPAT2' ENTERED AT 10:21:18 ON 04 MAY 2005

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L1         61648 S (SI(W)GE OR SIGE OR SILICON(W)GERMANIUM)
L2         34471 S (INSULATOR(6A)SUBSTRATE#)
L3         18737 S (GE OR GERMANIUM)(8A)(SURFACE#)
L4        343245 S (SI OR SILICON)(8A)(LAYER#)
L5          6067 S (BARRIER(W)LAYER#)(8A)(RESIST? OR IMMUN? OR INSUSCEPT?)
L6       5393271 S (HEAT? OR ANNEAL?)
L7         10024 S L3 AND (FORM? OR PRODUC? OR MANUFACTUR? OR CREAT?)
L8          5580 S L3 AND L6
L9            22 S L1 AND L2 AND L3 AND L4 AND L5 AND L6

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